A NEW DUAL-BRIDGE SOFT SWITCHING DC-TO-DC POWER CONVERTER FOR HIGH POWER APPLICATIONS

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I. INTRODUCTION

The full-bridge (buck-derived) DC/DC converter with isolation on the intermediate high frequency AC link has been the preferred topology in many applications. The main advantages of this topology include constant frequency operation which allows optimum design of the magnetic filter components, pulse width modulation (PWM) control, minimum voltage and current (VA) stresses and good control range and controllability. However, the increase in device switching losses as the frequency increases and the high voltage stress induced by the parasitic inductances following diode reverse recovery are major drawbacks of this topology.

Various soft switching schemes (ZVS and ZCS) have been proposed to improve the performance of hard switching converters. One topology, which achieves PWM control with resonant switching, is the full-bridge ZVS (FB-ZVS) PWM converter shown in Fig. 1. In this topology, the transformer leakage inductance and the device's output capacitance are effectively utilized to achieve ZVS. The load range can be extended by properly sizing the leakage inductance of the transformer. In order to ensure ZVS, enough energy needs to be stored in the leakage inductance of the transformer. Since the leakage energy is a function of the load current, ZVS will be lost below a certain load level for the lagging leg switches.

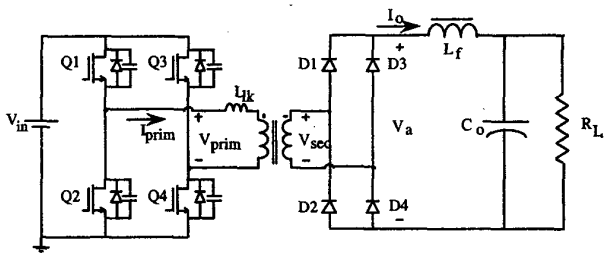

Fig. 1: Full Bridge ZVS PWM converter

In order to extend the zero voltage switching range of the full bridge converter, a variation of the circuit is the pseudo full bridge PWM ZVS converter, where an auxiliary inductor, L_a, is added to the lagging leg pole as shown in Fig. 2. In this case, additional energy is stored in the auxiliary inductance, which allows zero voltage turn-on for the lagging leg switches even at light loads. The penalty of adding an auxiliary inductor is the additional cost involved in addition to the winding losses incurred within the inductor winding. However, at high power levels, especially high output current levels, the incremental cost of such inductor is negligible while the savings in switching losses compensates the additional winding losses.

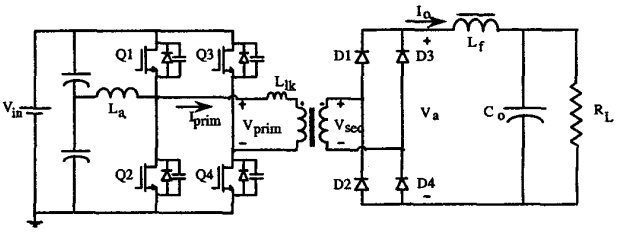

Fig. 2: Pseudo resonant full bridge ZVS PWM converter

One disadvantage of the pseudo, full bridge converter topology is susceptibility to shoot through in the case of gating the two switches of the same leg at the same time. If such a condition occurs, the switches will fail. Additional protection and control circuitry needs to be added to detect for such condition and disable the gating signals if the current in the devices exceeds a preset level. Such control action needs to be fast to prevent any possible faulty operation.

At high power levels, three-phase power is the most common form of power source available. In these cases, the input dc bus voltage is obtained by the use of a simple AC-to-DC rectifier bridge circuit as shown in Fig. 3. Due to the different voltage levels available at the different sites (230VAC, 460VAC,...), the DC bus voltage could be different as well. As an example, with a 230Vac three phase input voltage, the maximum DC bus voltage is 325Vdc while with a 460Vac input voltage, the dc bus voltage is 650Vdc. As a result, the DC-to-DC converter has to be designed

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specifically to match the input voltage source. This is due to the fact that the power switching devices have to be sized so as to operate safely at the prescribed DC bus voltage levels. For the above example, and since IGBTs are the most suitable devices at high power levels, 600V devices are needed for the 230Vac input voltage case while 1200V parts are needed for the 460Vac case.

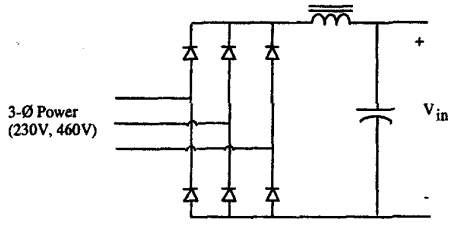


Fig. 3: AC-to-DC rectifier bridge

II. THE NEW PROPOSED CONVERTER TOPOLOGY

A new proposed converter topology based on the pseudo full bridge PWM ZVS converter has been developed. The new converter topology consists of two bridges that are coupled through an auxiliary coupled inductors, L_a and L_b, as shown in Fig. 4. Each bridge is based on the two switch forward converter topology. Since each switch is connected in series with a reverse conducting diode, no shoot through is possible and the topology is shoot through proof. In addition, the availability of two switching bridges provides the capability of connecting the two bridges in parallel for low line voltages (230Vac) and in series for high line voltage (460Vac) as shown in Figs. 5a and 5b. Hence, the same topology with the same devices can be used for different input line voltages. This is due to the fact that the devices voltage stress is the same for both cases.

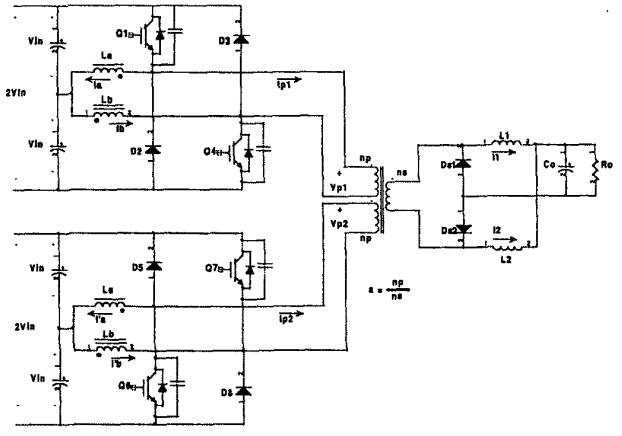
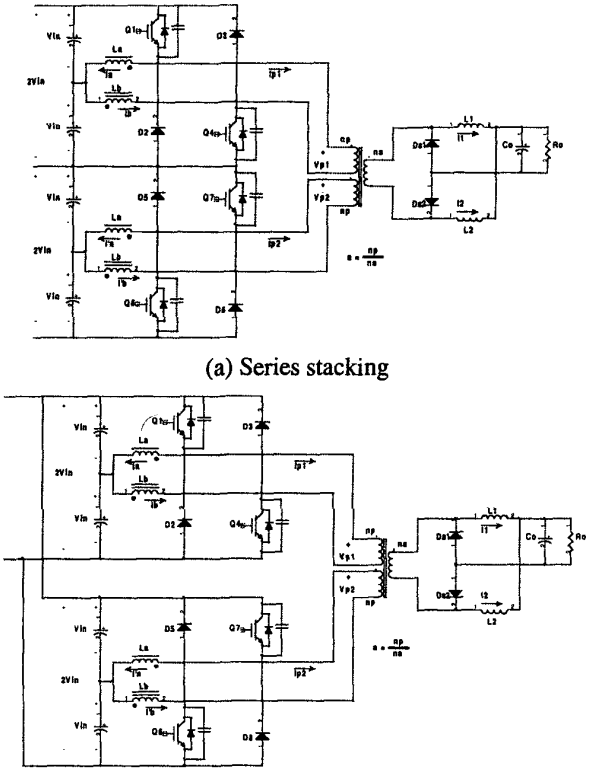


Fig. 4: The new DC-to-DC converter topology



(a) Series stacking

(b) Parallel stacking

Fig. 5: Series / Parallel stacking of the two bridges

As shown in Fig. 5, the two bridges are coupled through a set of coupled inductors, L_a and L_b. Each coupled inductor is connected such that it couples the pole of one bridge to the complementary pole of the other bridge. This allows the energy stored in the coupled inductor to commutate (charge the output capacitance of the turned off device and discharge the output capacitance of the incoming device) both poles of the converter bridges once a pole switch is turned off. This mechanism allows zero-voltage turn-on for all of the main switches and hence no turn-on losses. Using snubber capacitors across each switching device to slow down the rate of voltage rise across the device once it is turned off can minimize the turn-off losses. Note here that the energy stored in the coupled inductor should be enough to charge/discharge the device output capacitance in addition to the added snubber capacitance.

III. CONVERTER OPERATION

The converter is operated in a mode that provides zero voltage turn-on for the main devices. This is made possible by introducing a phase shift between the switches in the leading (right) legs and those in the lagging (left) legs of both bridges. The phase shift sets the duty cycle of the converter and hence the output voltage.

The operation of the converter topology will be explained next. Note here that the stacking of the two bridges (series or parallel) does not affect the operation of the converter.

Mode 1: $t_o \le t \le t_1$

With Q1 and Q4 initially conducting, Ds2 will be on with $V_{p1}=+2V_{in}$. The secondary filter current I_1 will ramp up while I_2 will ramp down linearly and power is delivered to the load. On the primary side, the voltage across the coupled inductor L_a is $+V_{in}$ and the current Ia ramps up linearly. In the same manner, the voltage across the coupled inductor L_b is $+V_{in}$ and the current Ib ramps up linearly as well. The equivalent circuit is shown in Fig. 6 (M1) and the corresponding waveforms during this mode are shown in Fig. 7.

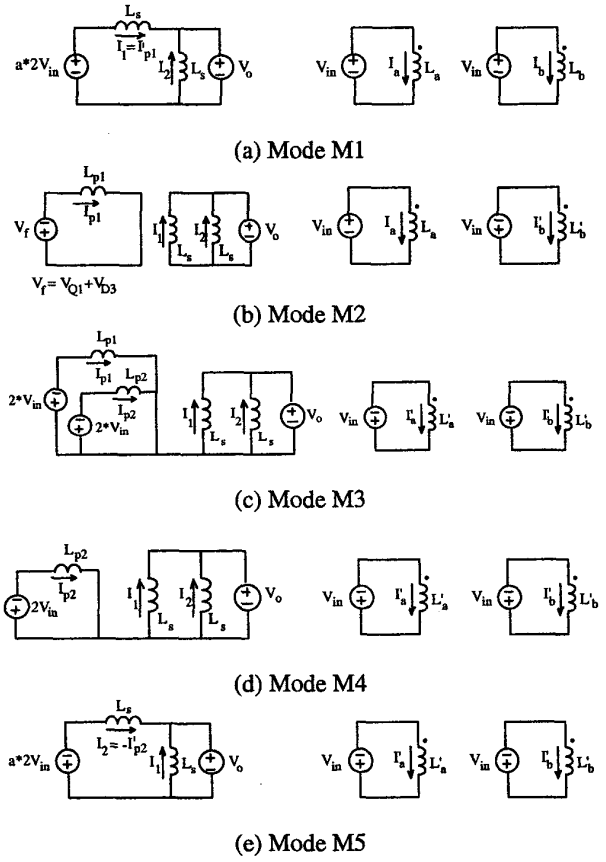


Fig. 6: Equivalent circuit modes

The governing equations during this mode are as follows,

$$I_1(t) = I_{1o} + \frac{a \cdot 2 \cdot V_{in} - V_o}{L_s} t \quad (1)$$

$$I_2(t) = I_{2o} - \frac{V_o}{L_s} t \quad (2)$$

$$I_p(t) = aI_1(t) \quad (3)$$

$$I_a(t) = I_{ao} + \frac{V_{in}}{L_a} t \quad (4)$$

$$I_b(t) = I_{bo} + \frac{V_{in}}{L_b} t \quad (5)$$

When Q4 is turned off, the energy stored in the output filter inductor L_1 will charge the output capacitance of Q4 and discharge the output capacitance of D3 causing D3 to conduct. The primary current will free wheel in Q1 and D3. Due to the coupling between L_b and L_b', the energy stored in the coupled inductor L_b will discharge the output capacitance of Q7 causing its anti parallel diode to conduct.

As a result, the voltage across the coupled inductor L_b will be $-V_{in}$ causing I_b to start ramping down linearly. The voltage across the transformer collapses to zero causing both diodes Ds1 and Ds2 to conduct. The time at which Q4 is turned off sets the duty cycle of the converter and hence controls the output voltage of the supply. This mode of control is referred to by phase shift control since the output power is controlled by varying the phase shift of the two converter poles with respect to each other.

Mode 2: $t_1 \le t \le t_2$

The equivalent circuit is shown in Fig. 6 (M2) and the corresponding waveforms during this mode shown in Fig. 7 (M2). In order to insure ZVS for Q7, a dead time is needed between the turn off of Q4 and the turn on of Q7 to insure that its anti-parallel diode conducts before it is turned on. The amount of dead time, Dt1, can be computed from,

$$I_b(t_1)\Delta t_1 = 4 \cdot C_{eff} V_{in} \quad (6)$$

where C_{eff} is the effective device output capacitance and $I_b(t_1)$ is the commutation inductor current at time t_1. The governing equations during this mode are given by,

$$I_1(t) = I_1(t_1) - \frac{V_o}{L_s}(t - t_1) \quad (7)$$

$$I_2(t) = I_2(t_1) - \frac{V_o}{L_s}(t - t_1) \quad (8)$$

$$I_a(t) = I_a(t_1) + \frac{V_{in}}{L_a}(t - t_1) \quad (9)$$

$$I_b(t) = I_b(t_1) - \frac{V_{in}}{L_b}(t - t_1) \quad (10)$$

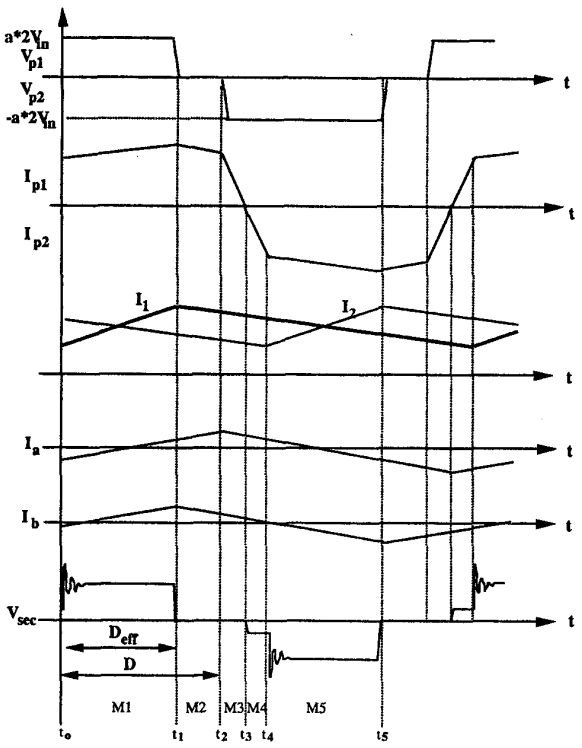


Fig. 7: Typical voltage and current waveforms of the converter

Mode 3: $t_2 \le t \le t_3$

Mode 2 is terminated by the turn off of switch Q1. As a result, the energy stored in the leakage inductance L_{p1} and part of the energy stored in the coupled inductor L_a will charge the output capacitance of Q1 and discharge the output capacitance of D2 causing D2 to conduct. Due to the coupling between L_a and L_a', the rest of the energy stored in the coupled inductor La will discharge the output capacitance of Q6 causing its anti parallel diode to conduct. As a result, the voltage across the coupled inductor L_a will be $-V_{in}$ causing Ia to start ramping down linearly. In addition, since the transformer primary side voltages $V_{p1}=-2V_{in}$ and $V_{p2}=2V_{in}$, the primary current I_{p1} ramps down to zero while I_{p2} ramps up linearly. On the secondary side, the output currents freewheels in Ds1 and Ds2. The equivalent circuit is shown in Fig. 6 (M3) and the corresponding waveforms during this mode shown in Fig. 7 (M3). The governing equations during this mode are given by,

$$I_1(t) = I_1(t_2) - \frac{V_o}{L_s}(t - t_2) \quad (11)$$

$$I_2(t) = I_2(t_2) - \frac{V_o}{L_s}(t - t_2) \quad (12)$$

$$I_a(t) = I_a(t_2) - \frac{V_{in}}{L_a}(t - t_2) \quad (13)$$

$$I_b(t) = I_b(t_2) - \frac{V_{in}}{L_b}(t - t_2) \quad (14)$$

In the above discussion, and due to the coupling arrangement, turning off a switch in one bridge causes part of the energy stored in the corresponding coupled inductor to discharge the output capacitance of the incoming device in the second bridge. Hence, zero voltage switching can be achieved over a wide load range by properly sizing the coupled inductors.

In order to ensure ZVS even at light loads, the energy stored in the commutation inductor should be higher than the energy stored in the device output capacitances, namely,

$$\frac{1}{2} \cdot L_b \cdot I_b^2(t_1) \ge \frac{1}{2} \cdot 2C_{eff} \cdot (2V_{in})^2 \quad (15)$$

$$\frac{1}{2} \cdot L_b \cdot I_b^2(t_2) \ge \frac{1}{2} \cdot 2C_{eff} \cdot (2V_{in})^2 \quad (16)$$

Mode 4: $t_3 \le t \le t_4$

When the primary side current I_{p1} reaches zero, mode 4 is initiated as shown in Fig. 6 (M4). At this stage, the primary current I_{p1} remains zero while I_{p2} starts ramping up linearly. During this mode, the output current keeps freewheeling through Ds1 and Ds2. When I_{p2} reaches the reflected secondary current I_2, Ds2 seizes to conduct and Ds1 takes over. This causes a voltage overshoot across Ds2 due to the diode reverse recovery and the energy stored in the transformer leakage inductance. The same overshoot occurs in full bridge converters with inductive output filters. Hence, the diodes Ds1 and Ds2 have to be derated and/or snubber circuits need to be used to limit the maximum voltage overshoot across them. Note that during this mode, a negative voltage is impressed across the main transformer, which resets the flux induced in the positive half cycle. The equivalent circuit is shown in Fig. 6 (M5).

The second half cycle is initiated by the turn off of Q6 and the converter goes through similar circuit modes as the positive half cycle.

IV. SIMULATION RESULTS

To verify the operation of the proposed converter topology, simulation results for a 12kW, 12V/1000A converter were obtained. The switching frequency was selected to be 35kHz. The main transformer primary-to-secondary turns ratio was set to 10:1. The commutation inductors used to ensure ZVS were 100 μH.

Figure 8 shows the resultant simulation results showing the different voltage and current waveforms of the converter. As expected, the primary voltages and currents match the expected waveforms shown earlier in Fig. 7. In addition, by investigating the main devices voltage and gating signals, it is clear that the voltage across the device is reset to zero first before the device is turned on. This is confirmed by the negative current flowing through the anti parallel diode of the device prior to turn on. Note here that the delay time, Δt, to guarantee ZVS was set to be 1μs.

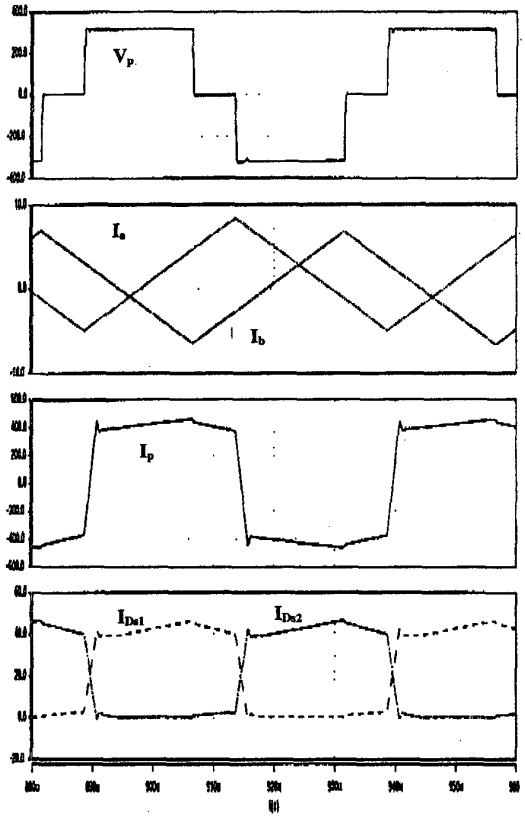


Fig. 8: Simulation results of the 12V/1000A unit at 5V/800A output

V. EXPERIMENTAL VERIFICATION

A 1000A/12V DC power supply with 230Vac input line was constructed and tested. Due to the low line voltage, the two bridges where connected in parallel. As a result, the DC bus voltage was 325 Vdc. Readily available 600V/75A IGBTs where used in this application. The main transformer primary-to-secondary turns ratio was set to 10:1. Schottky diodes were used on the secondary side due to their low forward drop. The coupled inductor was constructed using ferrite cores and litz wire. In order to guarantee ZVS even at light loads, 20 turns were used to wind the coupled inductors which resulted in a magnetizing inductance of approximately 100 μH. As a result, the rms current in the coupled inductor is nearly 4A which is only 5% of the primary current. Two 30μF dc blocking capacitors where used to block any dc current component in the coupled inductors.

The experimental results for the same unit are shown in Fig. 9-12. The primary current and voltage waveforms are shown in Fig. 10 while the commutation inductor current and voltage waveforms are shown in Fig. 11. The experimental waveforms match closely both simulations and expected ones.

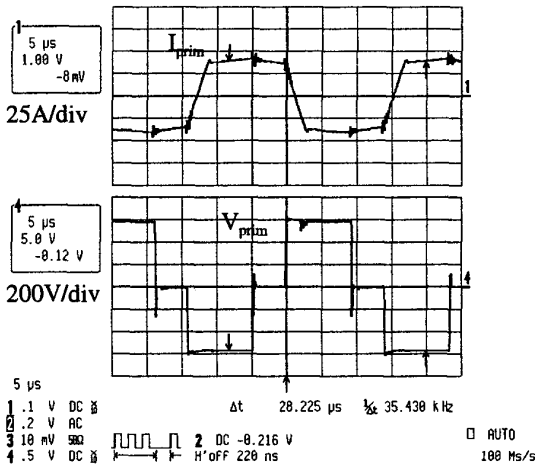


Fig. 9: Primary voltage and current

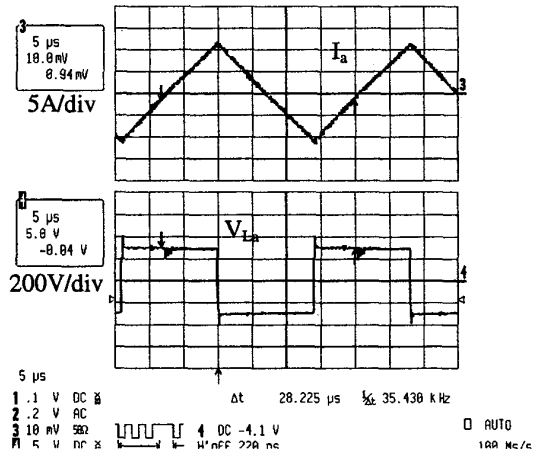


Fig. 10: Coupled inductor voltage and current

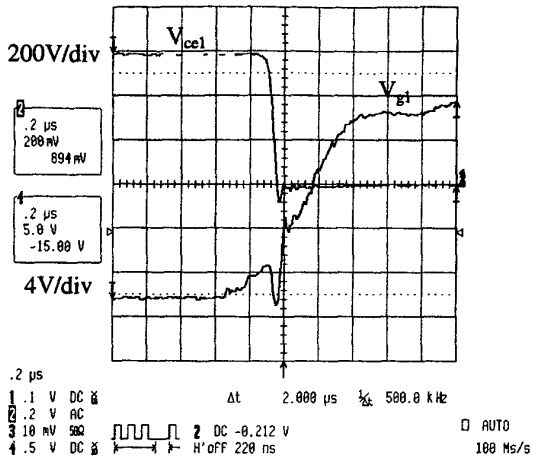


Fig. 11: Soft switching for lagging leg IGBTs

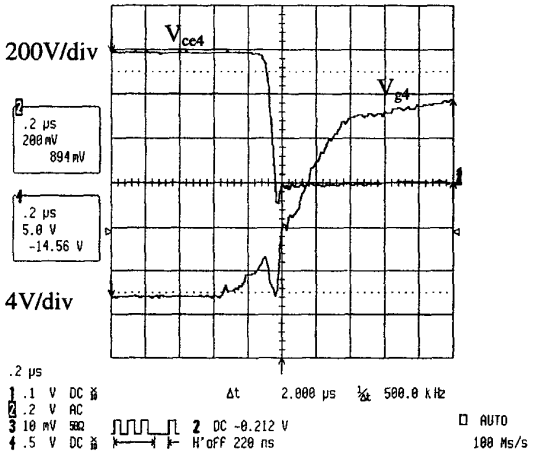


Fig. 12: Soft switching for leading leg IGBTs

VI. CONCLUSIONS

This paper has presented a dual bridge high current DC-to-DC converter with soft switching capability. The proposed dual bridge power supply is based on the two switch isolated forward converter. Unlike conventional dual bridge forward converters, phase shift control is employed to regulate the output voltage and achieve soft switching. Coupled transformers are utilized to achieve and maintain soft switching for the main devices over a wide load range. The availability of two switching bridges provides the capability of connecting the two bridges in parallel for low line voltages (230Vac) and in series for high line voltages (460Vac). This allows the use of low voltage rated switching devices for both low and high line applications. Furthermore, due to the bipolar excitation of the high frequency power transformer, the input capacitors are automatically balanced when the two bridges are connected in series.

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