SOFT SWITCHING INVERTER POWER SOURCE FOR ARC WELDING

H. Mecke, W. Fischer, F. Werther

Otto-von-Guericke-University Magdeburg, Institute ELE, Germany

Abstract. Modern electronic power sources for arc welding are mostly based on the inverter principle. The increase of switching frequency to about 100 kHz is desirable for further improvement of control capabilities and to reduce dimensions and weight and can only be reached sufficiently with soft switched semiconductors. A new control method has been developed for the ZVZCS - PS - FB - converter considering the specific static and dynamic load conditions of arc welding. Simulation results and experimental verification give good operation conditions over the entire load range.

Keywords. arc welding power source, soft switching, PS - ZVZCS - FB - converter, load adapted control

INTRODUCTION

Electronic controlled power sources are widely used in the industrial application of different arc welding processes. The increase of the switching frequency from 50 Hz of a phase controlled rectifier to about 20...60 kHz of a modern transistor controlled inverter allowed to reduce weight and dimensions of arc welding power sources dramatically. Furthermore, a precise control of the arc welding process with its complexity of heat input, material transfer and arc behaviour could be achieved [1]. For example, during striking of the arc there are two conditions with different requirements to the power source, the no load voltage of about 50 V and the rapidly rising arc current. To achieve controlled droplet transfer it is necessary to switch the current level from about 20A to 500A within less than 200 µs for a pulse time of 1 ms and a pulse frequency of 200 Hz.

Today the asymmetrical half-bridge-forward-converter became the favourite topology of an inverter power source. For higher output power, two stages are used in parallel, at the dc-input and the dc-output with 180° phase-shifting [2]. Hard switched IGBTs or MOSFETs with dissipative snubbers are mostly used as power switches dependent on supply voltage and output power range.

The switching losses limit the useable switching frequency. For this reason, the reduction of switching losses with resonant or soft switching topologies are necessary.

Arc welding power sources have to keep some requirements with regard to reduction of switching losses, that results from the characteristic of an arc welding process:

- extremely wide load range from no load to short circuit conditions
- extremely wide control range of load current to influence the welding process
- realisation of fast load current changes

From these requirements it is recognisable, that the mode of operation of the snubbers must be independent from the load conditions to operate entire without any switching losses.

As our investigation based on simulation results have shown conventional resonant and soft switching topologies are partly connected with considerable drawbacks like:

- switching losses at turn-off, resonant effects (series resonant converter above resonance) [3], [4]
- difficulties in achieving a wide power range without any switching losses (quasiresonant ZCS) [5]
- high expenditure due to auxiliary circuits (multiresonant ZCS, ZVT) [7], [8]
- low load currents (ZCS-PS-FB-converter) [6]

CIRCUIT TOPOLOGY AND BASICS OF OPERATION

A new topology that meets the requirements of arc welding with its dynamically changing load conditions is the PS-ZVZCS-FB-converter as introduced in [8], Fig.1.

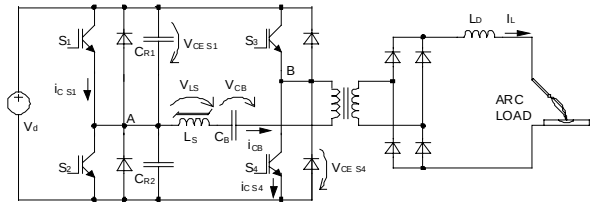

Fig. 1: Circuit topology of a PS - ZVZCS - FBC with arc load [8]

With this circuit based on a full bridge topology it is possible to control the primary voltage of the transformer by shifting the phase between the two halfbridge legs. In contrast to the standard ZVS-PS-FB-converter a saturable inductance and a blocking capacitor are connected in series with the transformer. Only two parallel connected capacitors across the transistors of one leg are necessary, instead of four capacitors in the standard topology. The basic idea of the control method is to achieve ZVS conditions for one leg and ZCS conditions for the other [8].

Fig.2 shows the standard control diagrams [8] and idealised switching waveforms at high load current from the PS-ZVZCS-FBC with arc load, assuming ideal switches S_1 - S_4 and diodes D_1 - D_4, an idealised transformer with a discrete leakage inductance L_{TrL} at the primary side, an ideal saturable inductor L_S (without hysteresis, two switching conditions with a linear characteristic) and a constant load current I_L. These waveforms can be divided into seven characteristic intervals to analyse circuit operation in the bridge diagonal for both directions (S1/S4, S2/S3).

Time interval T1 ($t_0 \le t \le t_1 \equiv \Delta t_1$):
At the time t_0 the transistor S_1 is turned on, while the transistor S_4 was already switched on. The still unsaturated inductor L_S ($L_S >> L_{TrL}$) limits the rise of the transistor current i_{CS4} at a very low value. A soft turn-on is achieved in this way. The intermediate circuit d.c. voltage is across the saturable inductor now and the ferrite core becomes saturated. T1 is finished when L_S is saturated.

Time interval T2 ($t_1 \le t \le t_2 \equiv \Delta t_2$)
The current i_{CB} is rising linearly towards the reflected output current $i_{CB} = I'_L = I_L/m$, limited through the leakage inductance of the transformer L_{TrL}.

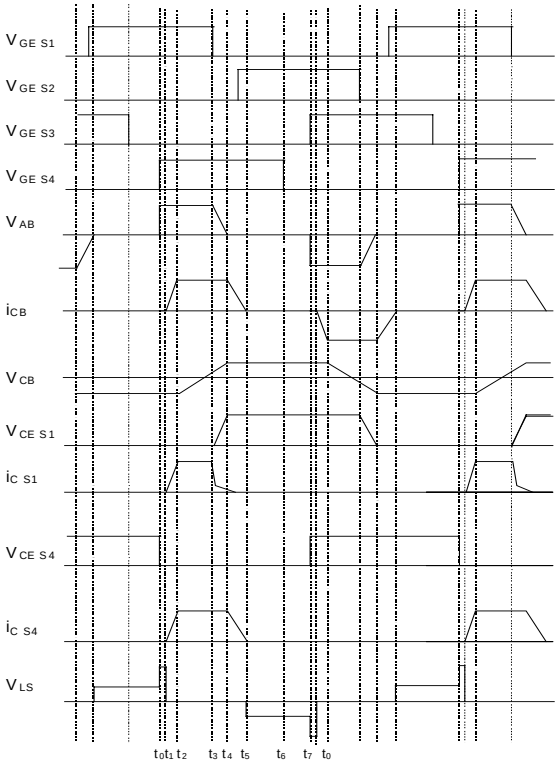

Fig. 2: Control diagram and switching waveforms at nominal load conditions

Time interval T3 ($t_2 \le t \le t_3 \equiv \Delta t_3$)
During T3 the energy transfer from of the intermediate d.c. circuit into the load takes place. The voltage across the blocking capacitor C_B is rising nearly linearly from $-V_{CBm}$ to $+V_{CBm}$. The capacitor can block any occurring d.c. voltage across the transformer by storing the energy differences. That could be a result from unequal overlap angles between the on - times of the transistors in both bridge diagonals ($\alpha_{S1/S4}$ in relation to $\alpha_{S2/S3}$). T3 is finished when S_1 is turned off.

Time interval T4 ($t_3 \le t \le t_4 \equiv \Delta t_4$)
The snubber capacitors C_{R1} / C_{R2} are charged/ discharged by the current i_{CB} beginning at the time t_3. For this reason the rise of the transistor voltage is limited and the transistor is turning off softly. The energy transfer is completed, when the secondary transformer voltage gets below the output load voltage. The freewheeling period begins at this time and the transformer is being shorted. The time interval T4 is finished when D_2 is conducting.

Time interval T5 ($t_4 \le t \le t_5 \equiv \Delta t_5$)
The voltage across the transistor S_2 is clamped at zero by the diode D_2. The transistor S_2 can be turned on with zero voltage across it (ZVS). The voltage V_{CBm} appears across the inductors L_{TrL} and L_S (saturated). Therefore the primary current is falling linearly. The time interval T5 is finished when the diagonal current i_{CB} turns back its direction and D_2 turns-off as a result.

Time interval T6 ($t_5 \le t \le t_6 \equiv \Delta t_6$)
The inductor L_S is not saturated any more. Therefore it is blocking the diagonal current on very low values and the discharge of the blocking capacitor is prevented. The transistor S_4 can be turned off with a current close to zero (ZCS). The time interval is finished when S_4 is turned off.

Time interval T7 ($t_6 \le t \le t_7 \equiv \Delta t_7$)
This time interval is necessary to allow the recombination of the remaining charge carriers at the inner p.n.-junction of the IGBT S_4. The transistor reaches its blocking capability faster than without ZCS. The interval is finished when S_3 is turned on.

BASIC DESIGN CONSIDERATIONS

Snubber capacitors

The snubber capacitor design is from a decisive importance for the effectiveness of the turn-off switching loss reduction for the transistors S_1 and S_2 and for the controllability of the inverter. The turn-off switching losses P_{VSoff} can be calculated for the transistors S_1/S_2 as a function of C_R assuming that the transistor current is falling linearly, Fig. 3.

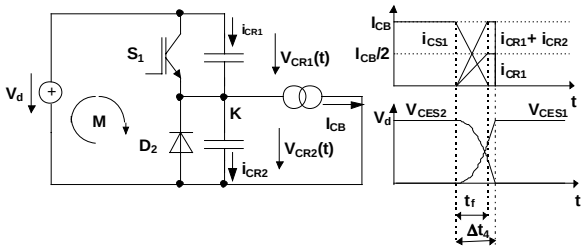

Fig. 3: Equivalent circuit for turn-off switching loss reduction at transistor S_1

Two cases are to be distinguished:

(1) $C_R > C_{Rcrit}$:
(The snubber capacitor voltage reaches the intermediate circuit d.c. voltage after i_{CS1} has reached zero.)

$$P_{VS1off} = W_{VS1off} f_S = \frac{I_{CB}^2 t_f^2}{48 C_R} f_S$$

(2) $C_R < C_{Rcrit}$:
(The snubber capacitor voltage reaches the intermediate circuit d.c. voltage before i_{CS1} has reached zero.)

$$P_{VS1off} = \frac{I_{CB}^2 t_f^2}{48 C_R} f_S \left[\frac{V_d C_R}{I_{CB} t_f} \left(28 + 96 \left(\frac{V_d C_R}{I_{CB} t_f} - \frac{1}{I_{CB}} \sqrt{\frac{V_d C_R I_{CB}}{t_f}} \right) \right) \right]$$

$$C_{Rcrit} = \frac{I_{CB} t_f}{4 V_d}$$

t_f - fall time of the transistor current
V_d - intermediate circuit d.c. voltage

Fig. 4 shows the calculated switching losses P_{VSoff} for both cases versus the capacitance of the snubber capacitors. It is obvious that the reduction of turn-off switching losses with $C_R >> C_{Rcrit}$ is insignificant. Therefore it is most suitable to design $C_{R1} = C_{R2} \approx C_{Rcrit}$.

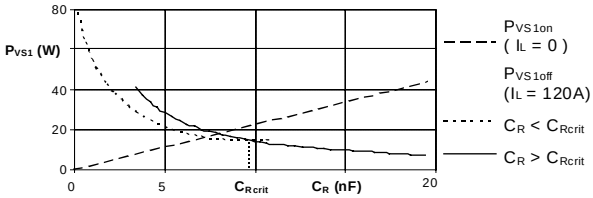

Fig. 4: Calculated switching losses of S_1 (IRGPC50U)
(t_f = 320 ns - collector current fall time)

Saturable inductor

The saturable inductor is required to prevent the discharge of the blocking capacitor during the time intervals $\Delta t_6 + \Delta t_7$ and to limit the current rise after the transistors S_3/S_4 are turned on. For this reason it is not allowed that the inductor saturates during these time intervals. The ferrite core cross-

sectional area A_{eLS} and the number of windings N_{LS}, required for this conditions, can be calculated as an approximate value from the linearisied inductor voltage waveforms during the time intervals $\Delta t_6 + \Delta t_7 + \Delta t_1$, Fig. 2.

$$A_{eLS} N_{LS} = \frac{V_{CBm\max}\left(\Delta t_6 + \Delta t_7\right) + \left(V_d + V_{CBm\max}\right)\Delta t_1}{B_{satLS}}$$

B_{satLS} - saturation flux density of ferrite core

Blocking capacitor

The diagonal current fall time depends on the leakage inductance value, the overlap angle between the on-times (means Δt_3+Δt_4), the saturable inductor and the blocking capacitor.

$$\Delta t_5 = \frac{2 C_B \left[L_{Ssat} + L_{TrL}\right]}{\Delta t_3 + \Delta t_4}$$

The maximum voltage across the blocking capacitor can be calculated as a function of output current:

$$V_{CBm} = \frac{I_L \left(\Delta t_3 + \Delta t_4\right)}{2\, m\, C_B}$$

The maximum voltage across the blocking capacitor V_{CBm} must be low to reduce ferrite core cross-sectional area of the saturable inductor. The blocking capacitor should be designed as a compromise between a relatively low maximum voltage across the blocking capacitor V_{CBm} and a short diagonal current fall time Δt_5. For this reason a small leakage inductance of the transformer is mostly important.

Control function

For the design of the closed-loop current control and for the selection of an appropriate driving pulse pattern it is of great importance to describe the dependence of the adjustable overlap time t_{on} respectively the overlap angle α on the load current analytically. Considering the design of the passive components and assuming linearised waveforms according to the equivalent circuits in Fig. 5 the control function is to be found with:

$$\alpha = 360° \, T_{ON} \, f_S$$

$$\alpha = 360° \left[\frac{m^2}{2} \frac{V_{arc} + R_L \, I_L}{m V_d - R_i \, I_L} - f_S \left(\frac{2}{3} \sqrt{\frac{4 m V_d C_R t_f}{I_L}} - \frac{L_{TrL} \, I_L + m N_{LS} A_{eLS} B_{satLS}}{m V_d} \right) \right]$$

f_S - switching frequency
m - turns ratio
N_{LS} - number of turns of saturable inductor
A_{eLS} - core cross-sectional area of saturable inductor

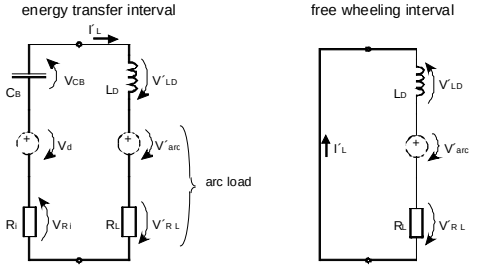

Fig. 5: Equivalent circuits for the calculation of the control function

Some of the calculated control characteristics are shown in Figure 6. They allow to estimate the influence of the passive components on the controllability of the load current. The influence of the snubber capacitors is of great importance for the control range of the power source. Their increase courses a decrease of the required overlap angle for a given load current because of the higher amount of the stored energy in these capacitors.

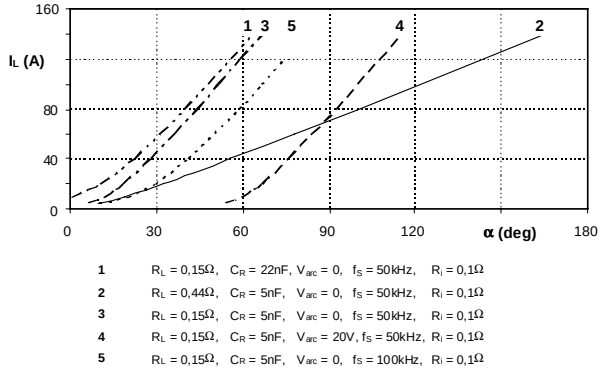

Fig. 6: Calculated control characteristics

With greater overlap angles the influence of the snubber capacitors decreases. Higher switching frequencies at the same load current require an increase of the overlap angle, because the time intervals Δt_1, Δt_2 and Δt_4 remain constant, while the time period of the control signal decreases. In this way, it becomes clear that a maximum switching frequency exists for a specific circuit design, output power and dimensioning of the passive components.

CONTROL METHOD

The development of an adapted control method for the PS-ZVZCS-FB-converter was an essential subject of research. A load-related control has to guarantee low-loss switching at the power transistors for all load conditions. The transistors S_1 and S_2 may only be turned on after the capacitors C_{R1} and C_{R2} were discharged completely. The discharge occurs through the load current reflected to the primary side. If the load current is on a low value this can take a relatively long time or if it is zero a discharge is impossible. While the next turn-on, the capacitors are discharged directly via the transistors. In this case the stored energy is converted into dissipative heat, depending on their capacitance, Fig. 4:

$$P_{VSon} = \frac{C_R \, f_S \, V_d^2}{2}$$

To avoid these losses it is necessary to adapt the control concept to the requirements of the arc load. For this purpose, the voltages across the snubber capacitors and across the output are checked. The driving pulse for the transistor S_1 or S_2 respectively, generated by the phase shift resonant controller (PSRC) is blocked until the corresponding capacitor C_{R1} or C_{R2} is discharged. This can be achieved very simply in the practical circuit design by blocking the driving stages of S_1/S_2.

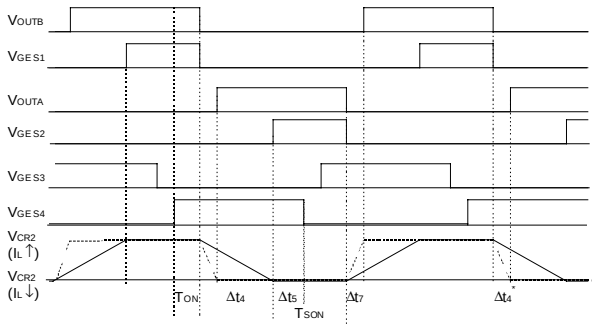

Fig. 7: On-times T_{SON} of the transistors S_1 and S_2 at different load currents

This modified control method is uncritical for the operation mode of the power source, because the time intervals necessary for the energy transfer and for transistor protection are not influenced negatively, Fig.7. At no load conditions, the capacitors are not discharged any more and the transistors S_1 and S_2 are not turned on, so that the circuit operates as a symmetrical half-bridge, Fig. 8. The current regulator generates a minimal overlap angle under these conditions.

The welding arc is ignited by a short contact between the welding electrode and the workpiece. This event is detected by a voltage sensor. If the arc voltage becomes lower than a reference value the blocking of the transistors S_1 and S_2 is deactivated. After a delay of some microseconds the current regulator operates at normal conditions to achieve a fast current rise without overshoot.

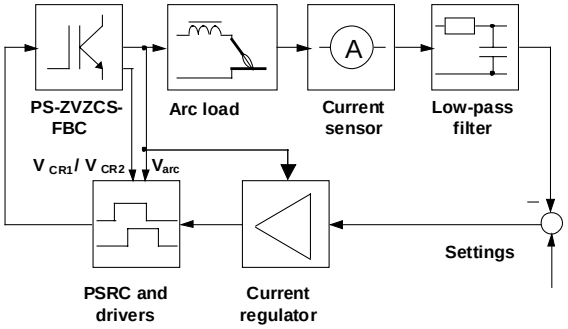

Fig. 8: Closed-loop adaptive current control (block diagram)

COMPUTER SIMULATION AND EXPERIMENTAL RESULTS

An experimental welding power source with a maximum output power of 3,5 kW with 230 V a.c. single phase line input has been built up to verify the correct operation mode of the newly developed control method, to analyse switching losses, efficiency and dynamic properties. The passive components of the experimental power source have been designed as follows:

$C_{R1} = C_{R2}$	=	7,5 nF	
C_B	=	1,32 µF	($V_{CBm} \approx 62$ V)
L_S	=	0,11 mH	($L_{Ssat} = 0{,}056$ µH)
L_{TrL}	=	3,7 µH	
m	=	4	

Fig. 9 shows the measured current and voltage waveforms at the output during a load transition from no-load to short circuit conditions without overshoot. Fig.10 shows the voltage waveforms across the transistors S_1 and S_4 and the current through S_4 after the welding electrode has touched the workpiece and before the current regulator and the drivers for S_1 and S_2 are released (transition from no-load to short-circuit).

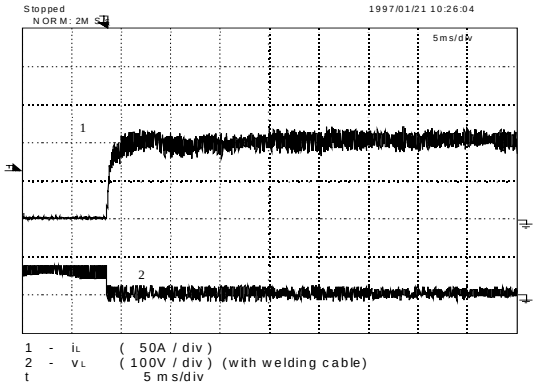

Fig. 9: Measured load current and voltage during transition from no-load to short-circuit

It is recognisable, that transistor S_4 operates with nearly no switching losses and the complete charge changes of the snubber capacitors C_{R1} and C_{R2} are also visible. The transistors S_1 and S_2 can turned on with ZVS in this case after their drivers are released.

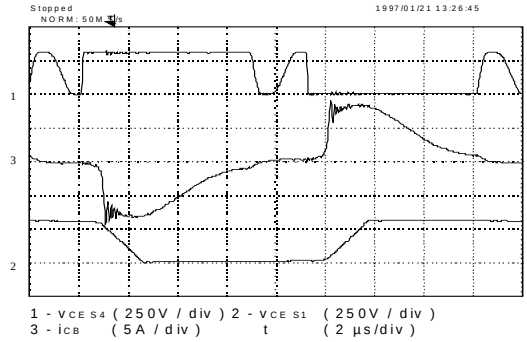

Fig. 10: Switching loss reduction of transistor S_4 when drivers of S_1/S_2 are blocked

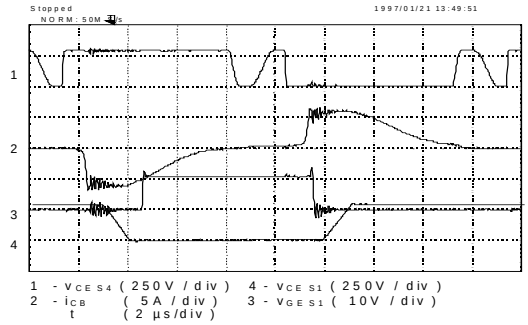

Fig. 11: Switching loss reduction of transistors S_1 and S_4 at low load conditions ($I_L = 30$ A)

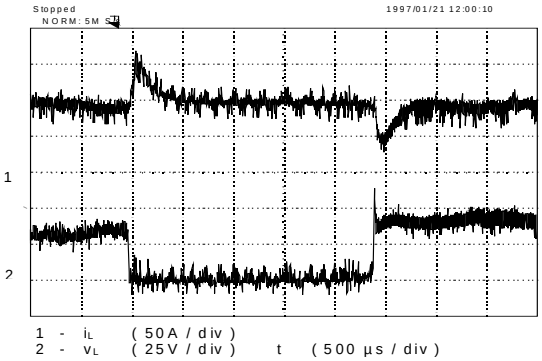

Fig. 12: Load current and voltage during transition from arc load to short-circuit and vice versa

Fig. 11 shows the adaptation of the driver signals of S_1 at lower load current (I_L = 30 A). Fig. 12 and Fig. 13 show the load current and voltage waveforms during a short time electrode short circuit with a following re-ignition of the arc. As experimental results have shown during all critical phases of dynamic load changes the control method guarantees a loss-less respectively a low-loss switching performance of all transistors.

The results of practical investigation have been confirmed by simulation. The used mixed-mode simulator SABER is suitable for the simulation of the power stage with IGBTs, control and load. The simulation system allows the adequate accurate reproduction of properties of the IGBT IRGPC50U by using its simulation model.

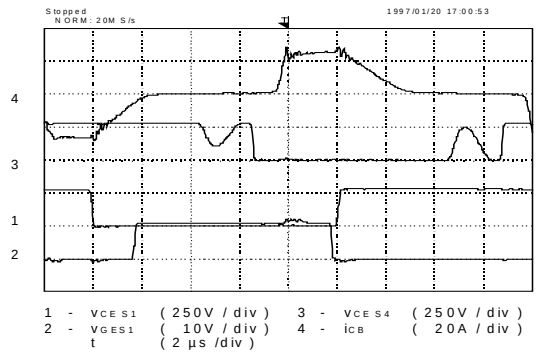

Fig. 13: Voltages across transistors S_1 and S_4 and primary transformer current at transition from short-circuit to arc load (zoomed from Fig. 12)

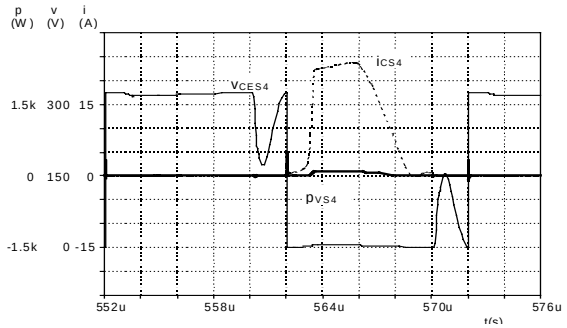

Fig. 14: Current, voltage and power waveforms of S_4 during transition from short-circuit to arc load (simulated)

Simulated and measured waveforms can be compared from Fig.13 - Fig. 15. The effect of switching losses reduction is recognisable from the simulated waveforms of power losses in the transistors. Merely small turn off switching losses in the transistors S_1 and S_2 are to be seen. The secondary rectifier-bridge and wiring causes relatively high power losses as shown in Fig. 16. The leakage inductance of the transformer limits the attainable switching frequency in this experimental power source.

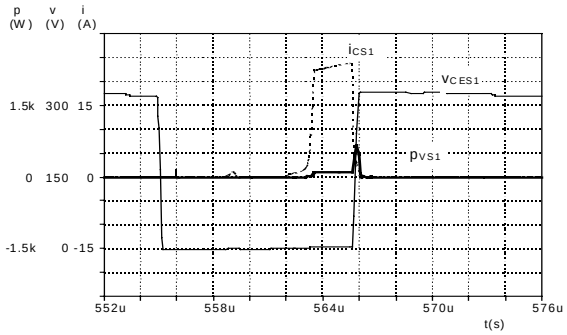

Fig. 15: Current, voltage and power waveforms of S_1 during transition from short-circuit to arc load (simulated)

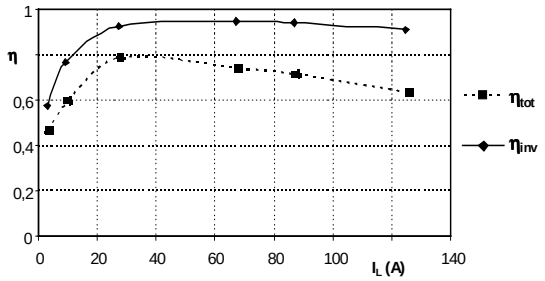

Fig. 16: Inverter and total efficiency of the experimental arc welding power source

The experimental power source realises a maximum output power P_{Lmax} = 3,5 kW and an efficiency η = 0,92 between 24% and 100% of the nominal load. It is possible to use IGBTs of the type IRGPC50U with a switching frequency between 50 kHz and 80 kHz, [9].

CONCLUSIONS

The PS-ZVZCS-FB-topology connected with the developed control method with a dynamic adjustment of the impulse sequence depending on load conditions makes it possible for the power transistors of an arc welding power source to operate with nearly no switching losses over the entire control and load ranges. Additional components on power stage are not required, compared to the topology that was presented in [8]. Measurements at an experimental power source and results from computer simulation verified, that the power transistors operate, even at fast load changes, with nearly no switching losses.

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Addresses of the authors

Prof. Dr.-Ing. habil. Hubert Mecke, Dr.-Ing. Wolfgang Fischer,
Dipl.-Ing. Frank Werther
Otto-von-Guericke-University Magdeburg
Institute of Electrical Engineering and Power Electronics (IELE)
P.O. Box 4120
D-39016 Magdeburg, Germany
Tel.: (+49 391) 67 18594
Fax.: (+49 391) 67 12408